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EXAMINER	
VAN ROY, TOD THOMAS	

ART UNIT	PAPER NUMBER
2828	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/803,042	ISHIDA ET AL.	
	Examiner	Art Unit	
	TOD T. VAN ROY	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The examiner acknowledges the amending of claims 1, 23, 30, and the cancellation of claim 2.

Response to Arguments

Applicant's arguments with respect to claims 1, and 2-31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

Claims 3, and 8-9 are objected to because of the following informalities:

These claims depend from cancelled claim 2, and are believed to more correctly depend from claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3-6, 9, 12-17, 18, 20-21, 23-28, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson in view of Kasai and Fischer (US 2003/0091076).

As for claim 1 Thompson teaches in figure 7, a laser modulating and driving device comprising: a modulation signal generating unit provided in a first block 32 configured to generate and output a laser modulation signal consisting of a pair of symmetrical (col.13 lines 25-41, complements) small swing differential signals (D1 and D2) based on pixel data (See abstract); and a driving unit provided in a second block spatially separated from the first block (30 and 24) and configured to drive a laser 12 according to the laser modulation signal output and supplied from the modulation signal generating unit; additionally, the modulation signal generating 32 unit has a modulation circuit configured to produce a modulation signal, and a small swing differential signal output circuit configured to convert the modulation signal to said pair of small swing differential signals D1 and D2, and the driving unit (30 and 24) has a small swing differential signal input circuit for receiving said pair of small swing differential signals (bases of 256). Thompson does not teach the high voltage of the small swing signal to be less than a supply voltage while the low voltage is greater than ground, or the blocks to be on different substrates. Fischer teaches a laser driver using differential signals (abs.) wherein the differential voltage levels are taught to be adjustable ([0034]). Kasai teaches a similar system in which the units are formed on separate substrates (fig.2, pc boards, col.7 lines 35-40). It would have been obvious to one of ordinary skill in the art

at the time of the invention to adjust the voltage levels from the supply and ground levels in order to avoid exceeding base-emitter biasing constraints on various types of transistors (Fischer [0034]) as well as to place the already separated units of Thompson onto individual substrates as taught by Kasai in order to organize the circuit components to conserve space as well as to thermally isolate the circuits to prevent overheating problems. (see also MPEP 2144.05 discussing separation of parts)

A reference noted, but not relied upon, is that of US 2003/0072339 which describes a laser driver using differential signals wherein adjustment of the voltage levels to desired values is taught ([0008]).

As for claim 3, the small swing differential signal output circuit includes: a non- inverted and inverted signal generating circuit configured to produce a non-inverted signal having the same phase as the modulation signal and an inverted signal with the phase shifted by 180 degrees from the modulation signal (see column 13 lines 32-35); and a small swing output circuit configured to reduce swings of the non-inverted signal and the inverted signal to output said pair of small swing differential signals as the laser modulation signal.

As for claim 4, wherein the small swing output circuit is formed as current mode logic (CML) or emitter coupled logic (ECL); see column 13 lines 2-6. Note the claim requires the circuit to be ECL or CML not the output.

As for claim 5, a reference potential of the ECL is a supply voltage VCC (+12V) of the modulation signal generating unit.

As for claim 6, a reference potential of the CML or ECL is an intermediate potential lower than a supply voltage VCC of the modulation signal-generating unit. There is current flowing through resistor 240 which would cause a drop in voltage from the supply voltage of +12V. Therefore the limitations of the claim are met.

As for claim 9 Thompson teaches, the small swing differential signal input circuit (30 and 24) has a differential signaling circuit-using transistors.

With respect to claims 12-14, Thompson teaches the apparatus outlined in the rejection to claim 1, including the spatially separation of the driving unit (fig.7 #30/24) from the modulating unit (fig.7 #32) via a transmission line (fig.7 D1/D2), and formation of a single integrated circuit (fig.7), and a pixel generating unit (fig.7 TTL to #250) configured to supply pixel data to the modulation unit (remainder of #32) formed on the same board.

As for claim 15, the modulation signal generating unit 32 has an output-stage inverter or buffer (236 or 232) having a supply terminal, to which a first voltage lower than a supply voltage (3.3 V) of the modulation signal generating unit is applied.

As for claim 16, the modulation signal generating unit 32 has an output-stage inverter or buffer (238 or 234) having a ground terminal, to which a second voltage higher than a ground voltage (3 V) is applied.

As for claim 17, the modulation signal generating unit has an output-stage inverter or buffer having a supply terminal (236,232,238, or 234), to which a first voltage lower (3.3 V) than a supply voltage of the modulation signal generating unit is applied (236 or

232), and a ground terminal (3V), to which a second voltage higher than a ground voltage is applied (238 or 234).

As for claim 20, Thompson teaches all that pertains to claim 1. Thompson further teaches, the modulation signal generating unit 32 is formed in a block spatially separated from the driving unit (30 and 24), and has an output-stage inverter or buffer (236 and 232 or 238 and 234) and a resistor 26 arranged outside the block to reduce a swing of an output of the output-stage inverter or buffer. The buffers 236, 232,238 and 234 are commercially available chips (74F14 and DS0056) and therefore would have to be outside the block. Therefore all the limitations of the claim are met.

As for claim 21, Thompson teaches all that pertains to claim 1. Thompson further teaches, the modulation signal generating unit 32 has an output-stage inverter or buffer (232 and 236 or 234 and 238) and a resistor (252 or 254) connected to an output from the output-stage inverter of buffer (the resistor is connected to the buffer, therefore the limitation is met) to reduce a swing of the output from the output-stage inverter or buffer (intended use), and the driving unit (30 and 24) has an input-stage differential signaling circuit using a transistor 256.

With respect to claims 23-24, Thompson and Kasai teach the device of claim 1, including a pixel data generating unit configured to produce pixel data (abs.) Thompson does not teach the unit to be additionally included on the first substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the pixel unit on the first substrate in order to minimize data loss which can occur over lengthy transmission lines.

Claim 25 is rejected for the same reasons as claim 2.

With respect to claim 26, as the two units are on separate blocks, the first block can be said to have a first logic, and the second block a second logic.

With respect to claim 27, Thompson teaches the first logic is ECL (col.13 lines 4-5).

With respect to claim 28, Thompson teaches the second logic is differential signaling using a pair of transistors (fig.7 near #256).

With respect to claims 30-31, Thompson and Kasai teach the device outlined in the rejection to claims 23-24, and additionally teach a photosensitive unit and a laser (fig.1).

Claims 8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, Kasai, Fischer, and further in view of Kaminishi (US 6618406).

As for claim 8 Thompson, Kasai, and Fischer teach all that pertains to claims. However they do not explicitly disclose that the input and output circuits of the small swing differential circuits use different supply voltages. Kaminishi teaches, "Since the control range of the DC bias current is large, here is used Vcc larger than Vcs as the power source of the amplifier. Furthermore... influences from changes and fluctuation in transistor characteristics and fluctuation in source voltage are alleviated."(Column 17 lines 25-34). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a larger Voltage (i.e. higher supply voltage) source for

the driver (input) than the modulation circuit (output) to have a large control range. Also it would have been obvious because fluctuations in the source voltage are alleviated.

As for claim 22, Thompson, Kasai and Fischer teach all that pertains to claim 1 respectively. However they do not disclose that the input and output circuits of the small swing differential circuits use different supply voltages. Kamanishi teaches, "Since the control range of the DC bias current is large, here is used Vcc larger than Vcs as the power source of the amplifier. Furthermore... influences from changes and fluctuation in transistor characteristics and fluctuation in source voltage are alleviated."(Column 17 lines 25-34). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a larger Voltage (i.e. higher supply voltage) source for the driver (input) than the modulation circuit (output) to have a large control range. Also it would have been obvious because fluctuations in the source voltage are alleviated.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, Kasai, Fischer, and further in view of Trotter et al. ("A CMOS low voltage high performance interface" Trotter, J.D. Rekhi, S. Chava, V. Kale, P.C.; Microsyst. Prototyping Lab., Mississippi State Univ., MS, USA; ASIC Conference and Exhibit, 1994. Proceedings. Seventh Annual IEEE International; 19-23 Sept. 1994; pgs 44- 48, Rochester, NY).

As for claim 10 and 11, Thompson, Kasai, and Fischer teach all that pertains to claim 1. Thompson further teaches, a signal transmission line (D1 or D2) configured to connect the modulation signal generating unit 32 and the driving unit (30 and 24),

through which said pair of small swing differential signals propagate (at D1 and D2). However Thompson does not disclose using parallel resistors at both ends of the transmission lines. Trotter teaches, "Parallel termination techniques with the voltage dividers (resistors) at each end of the bus matching characteristic impedance are preferred. In this case, there are no reflected waves (currents) and the initial signal is at full magnitude" (pg 47, second column 7th-3rd line from the bottom). Therefore it would have been obvious to terminate both ends with resistors (voltage dividers) to prevent reflection of the voltage.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, Kasai, Fischer, and further in view of Canright ("Practical design for controlled impedance" Canriqht, R.E., Jr. Martin Marietta Electron. Orlando, FL, USA; Electronic Components and Technology Conference, 1991. Proceedings. 41st: 11-16 May 1991; pgs. 370 - 377; Atlanta, GA).

As for claim 19, Thompson, Kasai, and Fischer teach the laser modulating and driving device of claim 1, wherein the modulation signal generating unit has an output-stage inverter or buffer. However they do not disclose a resistor in series with the buffer. Canright teaches "... even though the tolerance was allowed on the series termination resistor, the series termination produced a larger tolerance on Z0... Larger manufacturing tolerances are desirable" (pg 376 column 1 lines 2-7). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a

series resistor on the transmission line, D1 and D2 (which is in series with the buffer), to allow for a larger tolerance.

Allowable Subject Matter

Claims 7, 18, and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOD T. VAN ROY whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TVR

/AMIR ZARABIAN/

Supervisory Patent Examiner, Art Unit 2827